SwitchReg™

Dual Channel 600mA Step-Down Converter

General Description

The AAT2514 SwitchReg™ is a dual channel current mode PWM DC-DC step-down converter operating at 1.5MHz constant frequency. The device is ideal for portable equipment requiring two separate power supplies that need high current up to 600mA. The device operates from single-cell Lithium-ion batteries while still achieving over 96% efficiency. The AAT2514 also can run at 100% duty cycle for low dropout operation, extending battery life in portable systems while light load operation provides very low output ripple for noise sensitive applications.

The device has a unique adaptive slope compensation scheme that makes it possible to operate with a lower range of inductor values to optimize size and provide efficient operation. The 1.5MHz switching frequency minimizes the size of external components while keeping switching losses low. The AAT2514 can operate from a 2.5V to 5.5V input voltage and can supply up to 600mA output current for each channel.

The AAT2514 is available in a Pb-free, 3x3mm 10-lead TDFN package and operates over the -40°C to +85°C temperature range.

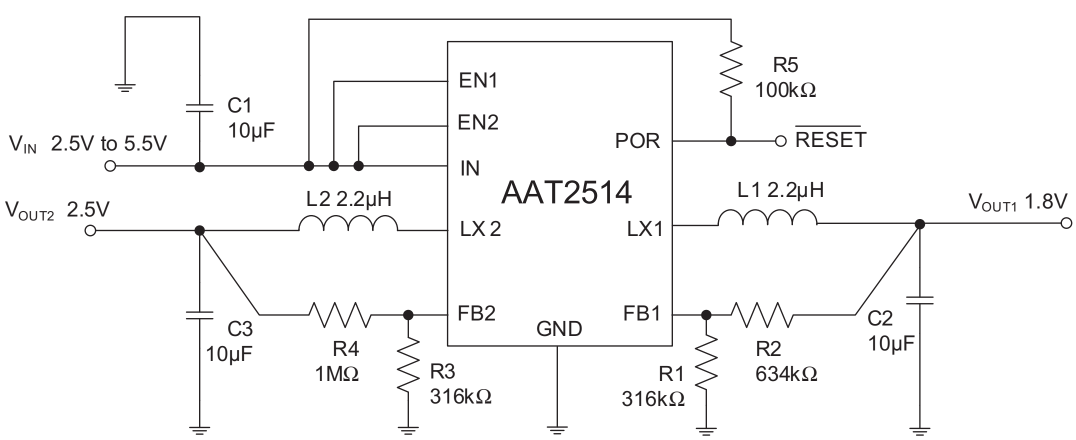
Features

- V_{IN} Range:2.5V to 5.5V
- Up to 600mA Output Current
- High Efficiency: Up to 96%
- 1.5MHz Constant Frequency Operation
- 100% Duty Cycle Dropout Operation
- Low $R_{DS(ON)}$ Internal Switches: 0.35Ω
- Current Mode Operation for Excellent Line and Load Transient Response
- Adaptive Slope Compensation
- Soft Start
- Short-Circuit and Thermal Fault Protection
- <1μA Shutdown Current
- Power-On Reset Output
- Small, Thermally Enhanced TDFN33-10 Package
- -40°C to +85°C Temperature Range

Applications

- Cellular Telephones
- Digital Still Cameras
- PDAs
- Portable Media Players
- Wireless and DSL Modems

Typical Application

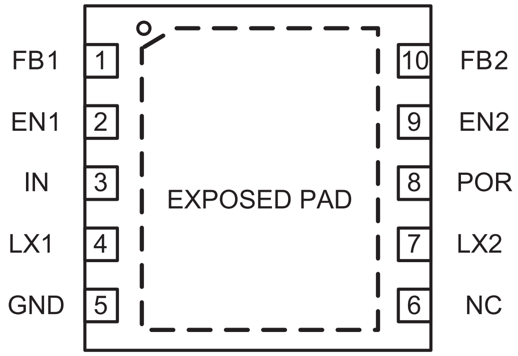


Pin Descriptions

Pin #	Symbol	Function
1	FB1	Feedback input for channel 1. Connect FB1 to the center point of an external resistor divider. The feedback threshold voltage is 0.6V.
2	EN1	Channel 1 enable pin. Active high. In shutdown, all functions are disabled drawing <1µA supply current. Do not leave EN1 floating.
3	IN	Power supply input pin. Must be closely decoupled to GND with a 2.2µF or greater ceramic capacitor.
4	LX1	Channel 1 switching node pin. Connect the output inductor to this pin.
5	GND	Ground.
6	N/C	No connection.
8	POR	Power-on reset, active low. Open drain. External resistor (100kΩ) is required.
9	EN2	Channel 2 enable pin. Active high. In shutdown, all functions are disabled drawing <1µA supply current. Do not leave EN2 floating.
10	FB2	Feedback input for channel 2. Connect FB2 to the center point of an external resistor divider. The feedback threshold voltage is 0.6V.
	EP	Exposed paddle. The exposed paddle should be connected to board ground plane and GND. The ground plane should include a large exposed copper pad under the package for thermal dissipation (see package outline).

Pin Configuration

AAT2514-IDE
TDFN33-10
(Top View)



10-Lead (3mm X 3mm) Plastic Thin DFN
Exposed Pad is PGND
Must be connected to GND.

Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	Input Supply Voltage	-0.3 to +6.0	V
V_{EN1}, V_{EN2}	EN1, EN2 Voltages	-0.3 to V_{IN} + 0.3	V
V_{FB1}, V_{FB2}	FB1, FB2 Voltages	-0.3 to V_{IN} + 0.3	V
V_{LX1}, V_{LX2}	LX1, LX2 Voltages	-0.3 to V_{IN} + 0.3	V
V_{POR}	POR Voltage	-0.3 to +6.0	V
T_A	Operating Temperature Range[2]	-40 to +85	°C
T_J	Junction Temperature[2]	+125	°C
$T_{STORAGE}$	Storage Temperature Range	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C

Recommended Operating Conditions

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance[3]	45	°C/W
P_D	Maximum Power Dissipation at T_A = 25°C	2.2	W

1. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
2. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \cdot \theta_{JA}$.
3. Thermal resistance is specified with approximately 1 square inch of 1 oz copper.

Electrical Characteristics

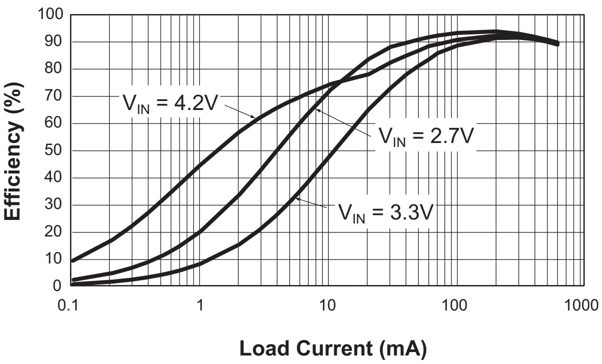
$V_{IN} = V_{EN} = 3.6V$, $T_A = 25°C$, unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
Step-Down Converter						
V_{IN}	Input Voltage Range		2.5		5.5	V
I_Q	Input DC Supply Current	Active Mode, $V_{FB} = 0.5V$		500	800	μA
		Shutdown Mode, EN1 = EN2 = 0V, $V_{IN} = 4.2V$		0.3	2.0	
V_{FB}	Regulated Feedback Voltage	$T_A = 25°C$, Channel 1 or 2	0.5880	0.6000	0.6120	V
		$T_A = 0°C \le T_A \le +85°C$, Channel 1 or 2	0.5865	0.6000	0.6135	
		$T_A = -40°C \le T_A \le +85°C$, Channel 1 or 2 (See Note 2)	0.5850	0.6000	0.6150	
I_{FB}	FB Input Bias Current		-30		30	nA
$\Delta V_{OUT}/V_{OUT}/\Delta V_{IN}$	Output Voltage Line Regulation	$V_{IN} = 2.5V$ to $5.5V$, $I_{OUT} = 10mA$		0.11	0.40	%/V
$\Delta V_{OUT}/V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation	$I_{OUT} = 10mA$ to $600mA$		0.0015		%/mA
I_{LIM}	Maximum Output Current	$V_{IN} = 3.0V$	600			mA
T_S	Startup Time	From Enable to Output Regulation		100		μs
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
F_{OSC}	Oscillator Frequency	$V_{FB} = 0.6V$	1.2	1.5	1.8	MHz
$R_{DS(ON)}$	P-Channel MOSFET	$I_{LX} = 300mA$		0.35	0.45	Ω
	N-Channel MOSFET	$I_{LX} = 300mA$		0.28	0.45	
	Peak Inductor Current	$V_{IN} = 3V$, $V_{FB} = 0.5V$; Duty Cycle <35%		1.20		A
$V_{EN(L)}$	Enable Threshold Low				0.3	V
$V_{EN(H)}$	Enable Threshold High		1.5			V
I_{EN}	EN Input Current		-1.0		1.0	μA
	Power-On Reset Threshold (POR)	V_{FB} Ramping Up		8.5		%
		V_{FB} Ramping Down		-8.5		
		Power-On Reset Delay		175		ms
		Power-On Reset On-Resistance		100		Ω

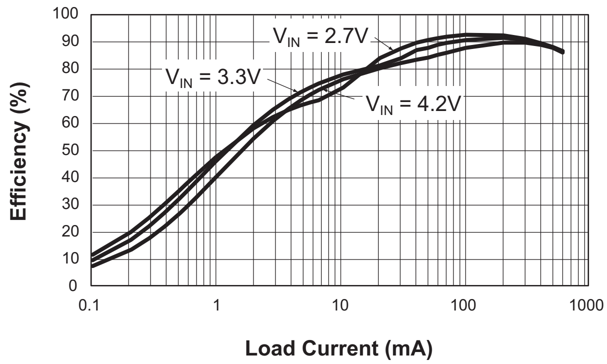
1. Specifications over the temperature range are guaranteed by design and characterization.
2. The regulated feedback voltage is tested in an internal test mode that connects V_{FB} to the output of the error amplifier.

Typical Characteristics

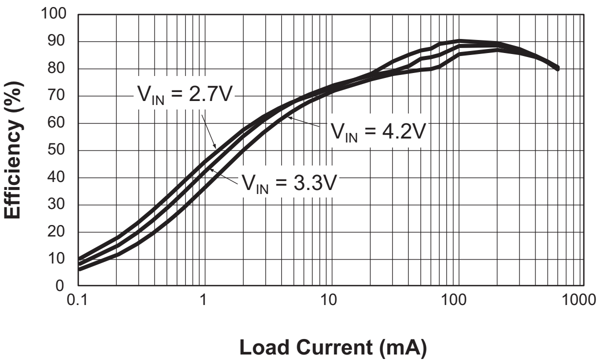
Efficiency vs. Load Current
(V_{OUT} = 2.5V; T_A = 25°C)



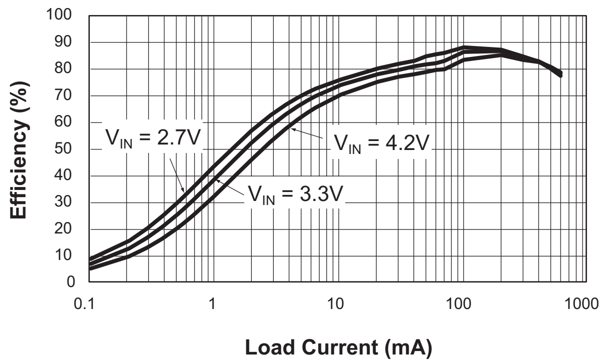
Efficiency vs. Load Current
(V_{OUT} = 1.8V; T_A = 25°C)



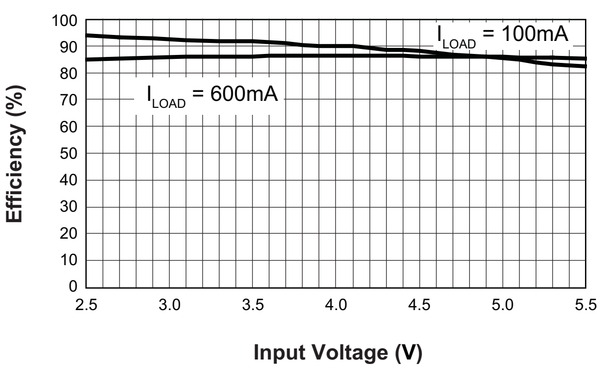
Efficiency vs. Load Current
(V_{OUT} = 1.5V; T_A = 25°C)



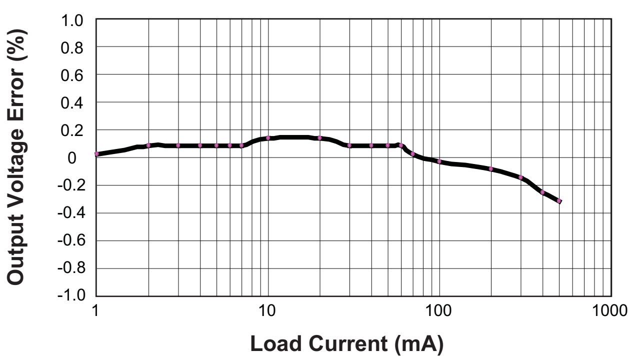
Efficiency vs. Load Current
(V_{OUT} = 1.2V; T_A = 25°C)



Efficiency vs. Input Voltage
(V_{OUT} = 1.8V; T_A = 25ºC)

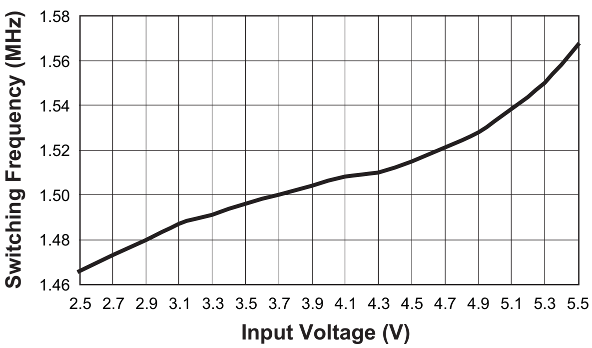


Load Regulation
(V_{IN} = 3.6V; V_{OUT} = 1.8V; L = 2.2µH)

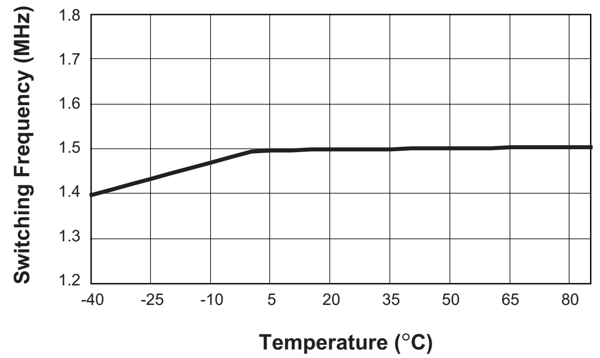


Typical Characteristics

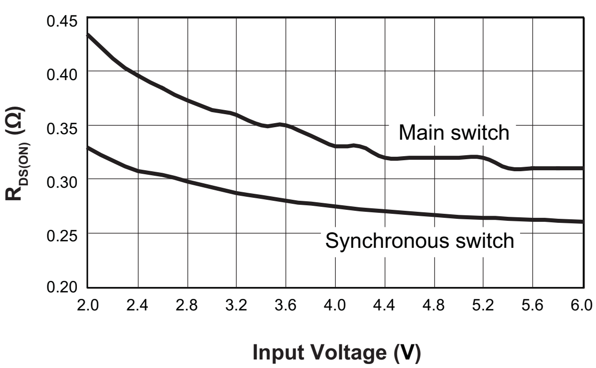
Frequency vs. Input Voltage
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{LOAD} = 150mA; L = 2.2µH)



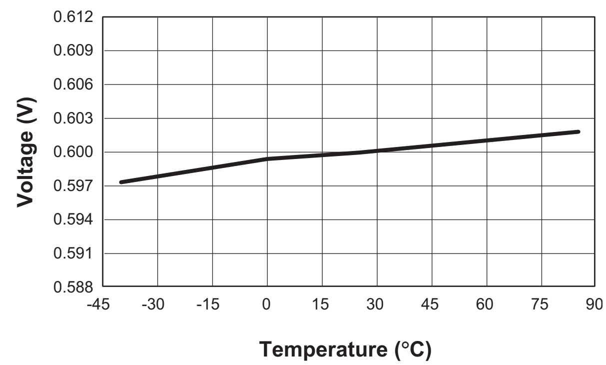
Frequency vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{LOAD} = 150mA; L = 2.2µH)



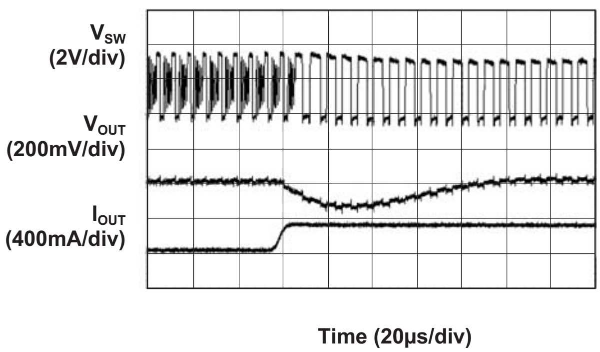
$R_{DS(ON)}$ vs. Input Voltage
(T_A = 25ºC)



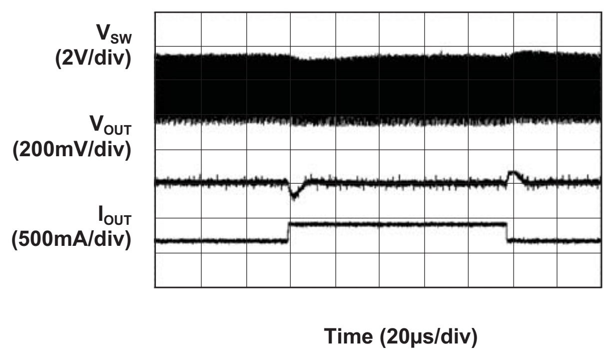
V_{FB} vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{LOAD} = 0mA)



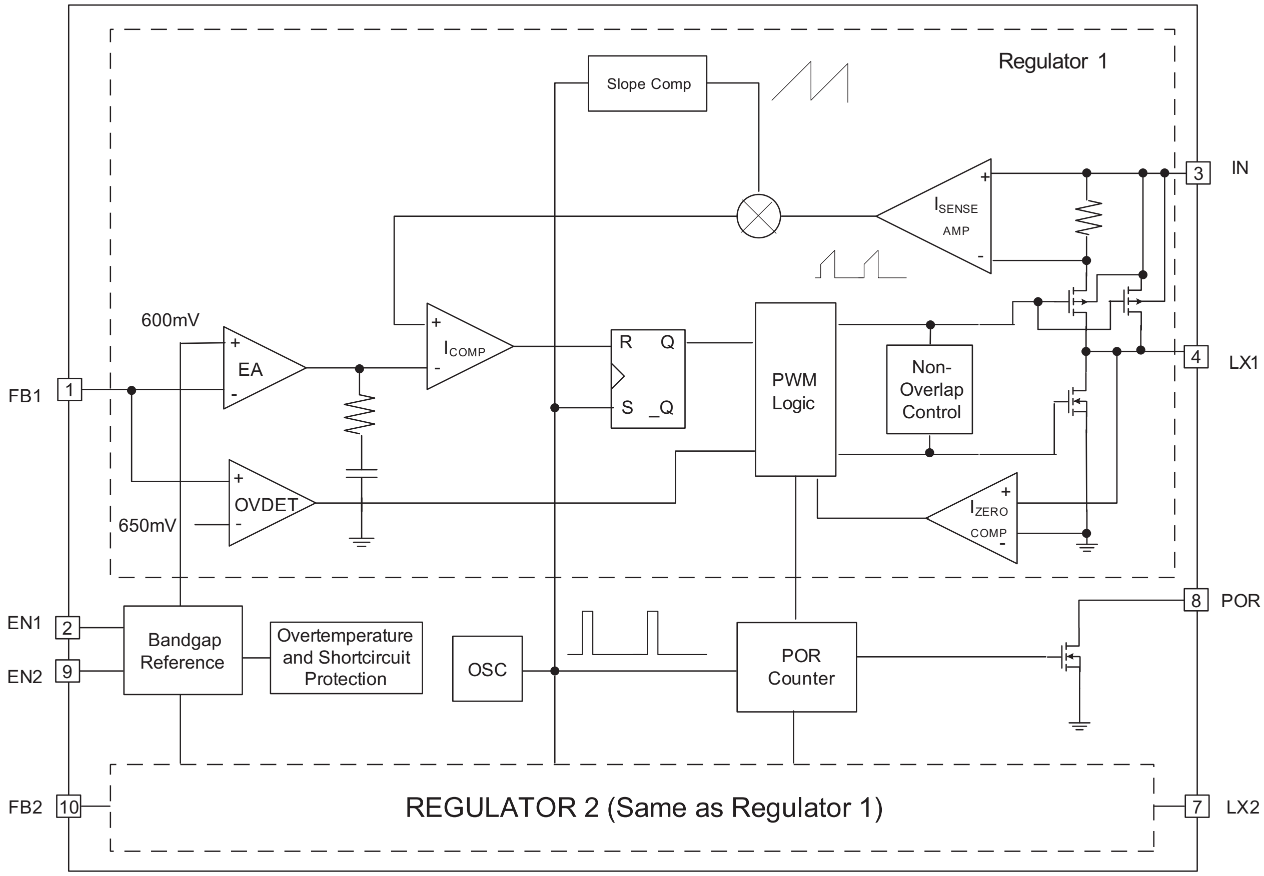
Load Transient Response
(Light Load Mode to PWM Mode; L = 2.2µH;
C_{IN} = 10µF; C_{OUT} = 10µF; V_{IN} = 3.6V; V_{OUT} = 1.8V)



Load Transient Response
(PWM Mode Only; I_{LOAD} = 180mA to 400mA; L = 2.2µH;
C_{IN} = 10µF; C_{OUT} = 10µF; V_{IN} = 3.6V; V_{OUT} = 1.8V)



Functional Block Diagram



Functional Description

The AAT2514 is a dual high performance 600mA, 1.5MHz fixed frequency monolithic switch-mode step-down converter which uses current mode architecture with an adaptive slope compensation scheme. It minimizes external component size and optimizes efficiency over the complete load range. The adaptive slope compensation allows the device to remain stable over a wider range of inductor values so that smaller values (1µH to 4.7µH) with associated lower DCR can be used to achieve higher efficiency.

Apart from the small bypass input capacitor, only a small L-C filter is required at each output. The adjustable outputs can be programmed with external feedback to any voltage, ranging from very low output voltages to the input voltage and by using an internal reference of 0.6V. The part uses internal MOSFETs for each channel to achieve high efficiency. At dropout, the converter duty cycle increases to 100% and the output voltages track the input voltage minus the low $R_{DS(ON)}$ drop of the P-channel high-side MOSFETs. The converter efficiency has been optimized for all load conditions, ranging from no load to 600mA at V_{IN} = 3V with an input voltage range from 2.5V to 5.5V. The internal error amplifier and compensation provides excellent transient response, load, and line regulation. Internal soft start eliminates any output voltage overshoot when the enable or the input voltage is applied.

Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for excellent load and line response and protection of the internal main switch (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET). During normal operation, the internal P-channel MOSFET is turned on for a specified time to ramp the inductor current at each rising edge of the internal oscillator, and is switched off when the peak inductor current is above the error voltage. The current comparator, I_{COMP}, limits the peak inductor current. When the main switch is off, the synchronous rectifier turns on immediately and stays on until either the inductor current starts to reverse, as indicated by the current reversal comparator, I_{ZERO}, or the beginning of the next clock cycle. The OVDET comparator controls output transient overshoot by turning the main switch off and keeping it off until the fault is no longer present.

Control Loop

The AAT2514 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short circuit and overload protection. An adaptive slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor. The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. For fixed voltage versions, the error amplifier reference voltage is internally set to program the converter output voltage. For the adjustable output, the error amplifier reference is fixed at 0.6V.

Enable

The enable pins are active high. When pulled low, the enable input forces the AAT2514 into a low-power, non-switching state. The total input current during shutdown is less than 2μA.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles. Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Dropout Operation

When the input voltage decreases toward the value of the output voltage, the AAT2514 allows the main switch to remain on for more than one switching cycle and increases the duty cycle until it reaches 100%.

The duty cycle D of a step-down converter is defined as:

$$D = T_{ON} \cdot F_{OSC} \cdot 100\% \approx \frac{V_{OUT}}{V_{IN}} \cdot 100\%$$

Where T_{ON} is the main switch on time and F_{OSC} is the oscillator frequency (1.5MHz).

The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor. At low input supply voltage, the $R_{DS(ON)}$ of the P-channel MOSFET increases and the efficiency of the converter decreases. Caution must be exercised to ensure the heat dissipated does not exceed the maximum junction temperature of the IC.

Maximum Load Current

The AAT2514 will operate with an input supply voltage as low as 2.5V; however, the maximum load current decreases at lower input due to the large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely, the current limit increases as the duty cycle decreases.

Applications Information

Setting the Output Voltage

Figure 1 shows the basic application circuit for the AAT2514. Resistors R1 and R3 and R2 and R4 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R1 and R3 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output voltages with R1 and R3 set to either 59kΩ for good noise immunity or 316kΩ for reduced no load input current.

The adjustable feedback resistors, combined with a external feed forward capacitors (C4 and C5 in Figure 1), deliver enhanced transient response for extreme pulsed load applications. The addition of the feed forward capacitor typically requires a larger output capacitor C2 and C3 for stability. The external resistor sets the output voltage according to the following equation:

$$V_{OUT} = 0.6V \cdot \left(1 + \frac{R2}{R1}\right)$$

or

$$R2 = \left[\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right] \cdot R1$$

V_{OUT} (V)	R1, R3 = 59kΩ R2, R4 (kΩ)	R1, R3 = 316kΩ R2, R4 (kΩ)
0.8	19.6	105
0.9	29.4	158
1.0	39.2	210
1.1	49.9	261
1.2	59.0	316
1.3	68.1	365
1.4	78.7	422
1.5	88.7	475
1.8	118	634
1.85	124	655
2.0	137	732
2.5	187	1000
3.3	267	1430

Table 1: Resistor Selection for Output Voltage Setting; Standard 1% Resistor Values Substituted Closest to the Calculated Values.

Inductor Selection

For most designs, the AAT2514 operates with inductor values of 1µH to 4.7µH. Low inductance values are physically smaller, but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{OSC}}$$

Where ΔI_L is inductor ripple current. Large value inductors lower ripple current and small value inductors result in high ripple currents. Choose inductor ripple current approximately 35% of the maximum load current 600mA, or ΔI_L = 210mA.

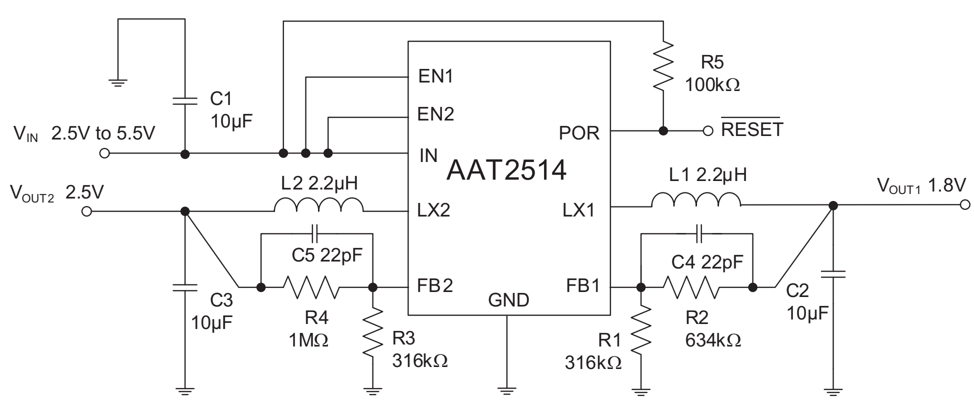


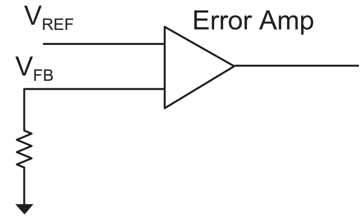
Figure 1: AAT2514 Typical Application Circuit.

For output voltages above 2.0V, when light-load efficiency is important, the minimum recommended inductor size is 2.2μH. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. For higher efficiency at heavy loads (above 200mA), or minimal load regulation (with some transient overshoot), the resistance should be kept below 100mΩ. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation (600mA + 105mA). Table 2 lists some typical surface mount inductors that meet target applications for the AAT2514.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor. For example, the 2.2μH CR43 series inductor selected from Sumida has a 71.2mΩ DCR and a 1.75ADC current rating. At full load, the inductor DC loss is 25mW, which gives a 2.8% loss in efficiency for a 600mA, 1.5V output.

Slope Compensation

The AAT2514 step-down converter uses peak current mode control with a unique adaptive slope compensation scheme to maintain stability with lower value inductors for duty cycles greater than 50%. Using lower value inductors provides better overall efficiency and also makes it easier to standardize on one inductor for different required output voltage levels. In order to do this and keep the step-down converter stable when the duty cycle is greater than 50%, the AAT2514 separates the slope compensation into 2 phases. The required slope compensation is automatically detected by an internal circuit using the feedback voltage V_{FB} before the error amp comparison to V_{REF}.



When below 50% duty cycle, the slope compensation is 0.284A/μs; but when above 50% duty cycle, the slope compensation is set to 1.136A/μs. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements.

Below 50% duty cycle, the slope compensation requirement is:

$$m = \frac{1.25}{2 \cdot L} = 0.284\text{A/μs}$$

Therefore:

$$L = \frac{0.625}{m} = 2.2\text{μH}$$

Above 50% duty cycle,

$$m = \frac{5}{2 \cdot L} = 1.136\text{A/μs}$$

Part	L (μH)	Max DCR (mΩ)	Rated DC Current (A)	Size WxLxH (mm)
CDRH2D11/HP	1.5	80	1.35	3.2x3.2x1.2
	2.2	120	1.10	
	3.3	173	0.9	
	4.7	238	0.75	
Sumida CDRH4D18	1.0	45	1.72	4.7x4.7x2.0
	2.2	75	1.32	
	3.3	110	1.04	
	4.7	162	0.84	
Toko D312C	1.5	120	1.29	3.6x3.6x1.2
	2.2	140	1.14	
	3.3	180	0.98	
	4.7	240	0.79	

Table 2: Typical Surface Mount Inductors.

Therefore:

$$L = \frac{2.5}{m} = 2.2\mu H$$

With these adaptive settings, a 2.2μH inductor can be used for all output voltages from 0.6V to 5V.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than the input source impedance to prevent high frequency switching current passing to the input. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

A low ESR input capacitor sized for maximum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22μF ceramic capacitor for most applications is sufficient. A large value may be used for improved input voltage filtering.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in Figure 3. A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q net-work that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result. Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem. In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

Output Capacitor Selection

The function of output capacitance is to store energy to attempt to maintain a constant voltage. The energy is stored in the capacitor's electric field due to the voltage applied.

The value of output capacitance is generally selected to limit output voltage ripple to the level required by the specification. Since the ripple current in the output inductor is usually determined by L, V_{OUT}, and V_{IN}, the series impedance of the capacitor primarily determines the output voltage ripple. The three elements of the capacitor that contribute to its impedance (and output voltage ripple) are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C). The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

In many practical designs, to get the required ESR, a capacitor with much more capacitance than is needed must be selected. For both continuous or discontinuous inductor current mode operation, the ESR of the C_{OUT} needed to limit the ripple to ΔV_O, V peak-to-peak is:

$$ESR \le \frac{\Delta V_O}{\Delta I_L}$$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes a temperature increase internal to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded. The output capacitor ripple current is the inductor current, I_L, minus the output current, I_O. The RMS value of the ripple current flowing in the output capacitance (continuous inductor current mode operation) is given by:

$$I_{RMS} = \Delta I_L \cdot \frac{\sqrt{3}}{6} \Delta I_L \cdot 0.289$$

ESL can be a problem by causing ringing in the low megahertz region but can be controlled by choosing low ESL capacitors, limiting lead length (PCB and capacitor), and replacing one large device with several smaller ones connected in parallel.

In conclusion, in order to meet the requirement of output voltage ripple small and regulation loop stability, ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current ratings. The output ripple V_{OUT} is determined by:

$$\Delta V_{OUT} \le \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot f_{OSC} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot f_{OSC} \cdot C3}\right)$$

A 10μF ceramic capacitor can satisfy most applications.

Thermal Calculations

There are three types of losses associated with the AAT2514 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode(CCM), a simplified form of the losses is given by:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DSON(HS)} \cdot V_O + R_{DSON(LS)} \cdot [V_{IN} - V_O])}{V_{IN}}$$

$$+ (t_{sw} \cdot F \cdot I_O + I_Q) \cdot V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_O^2 \cdot R_{DSON(HS)} + I_Q \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range. Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the MSOP-10 or DFN-10 packages, which is 45°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

Manufacturer	Part Number	Value	Voltage (V)	Temp. Co.	Case
Murata	GRM219R60J106KE19	10μF	6.3	X5R	0805
Murata	GRM21BR60J226ME39	22μF	6.3	X5R	0805
Murata	GRM1551X1E220JZ01B	22pF	25	JIS	0402

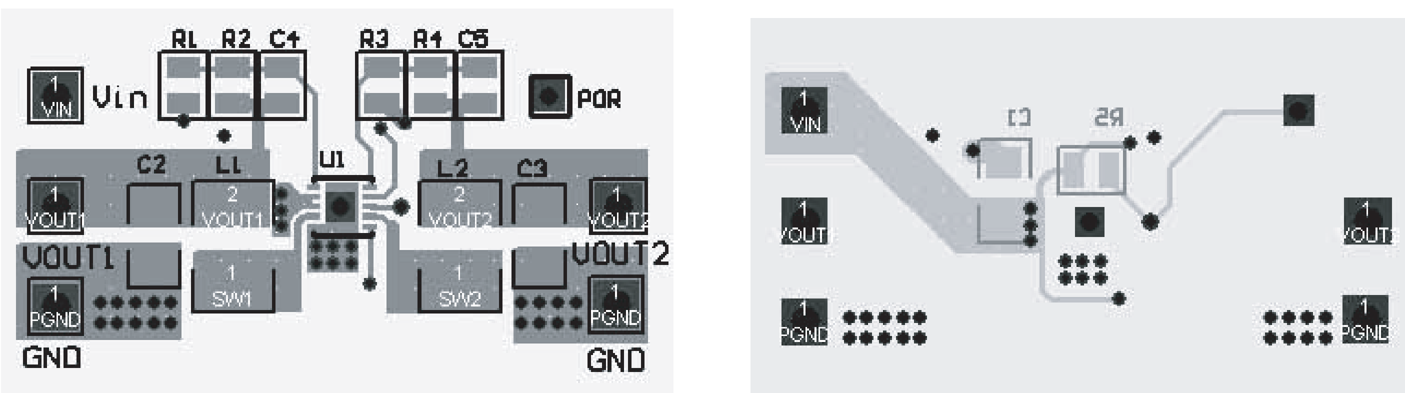
Table 3: Typical Surface Mount Capacitors.

Layout Guidance

Figure 1 is the schematic for a typical application. When laying out the PC board, the following layout guidelines should be followed to ensure proper operation of the AAT2514:

1. Exposed pad must be reliably soldered to GND. The exposed thermal pad should be connected to the board ground plane and GND. The ground plane should include a large exposed copper pad under the package for thermal dissipation.
2. The power traces, including the GND trace, the LX1/LX2 traces, and the VIN trace should be kept short, direct and wide to allow large current flow. The L1/2 connection to the LX1/2 pins should be as short as possible. Use several VIA pads when routing between layers.
3. The input capacitor (C1) should connect as closely as possible to IN and GND to get good power filtering.
4. Keep the switching nodes, LX1/LX2, away from the sensitive FB1/FB2 nodes.
5. The feedback traces or FB pins should be separate from any power trace and connected as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. The feedback resistors should be placed as close as possible to the FB pins to minimize the length of the high impedance feedback trace.
6. The output capacitors C2/C3 and L1/L2 should be connected as close as possible and there should not be any signal lines under the inductor.
7. The resistance of the trace from the load return to GND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

Figure 2 shows an example of a layout with 4 layers. The 2nd and 3rd layers are Internal GND Plane.



a: Top Layer *b: Bottom Layer*

Figure 2: AAT2514 Typical Application Circuit Layout.

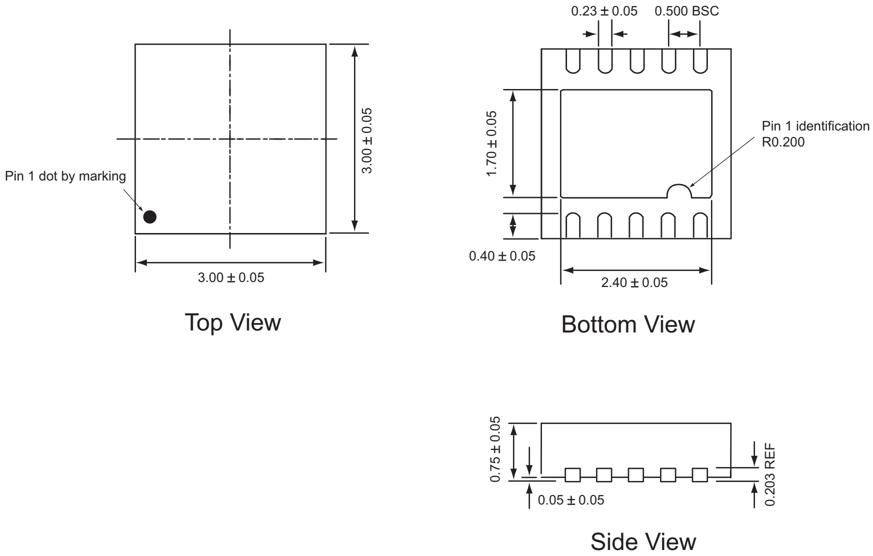
Ordering Information

Output Voltage[1]	Package	Marking[2]	Part Number (Tape & Reel)[3]
Adj. 0.6V to V_{IN}	TDFN33-10	ZBXYY	**AAT2514IDE-AA-T1[4]**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/aboutus/quality.php.

Package Information[5]

TDFN33-10



All dimensions in millimeters.

1. Please contact Sales for other voltage options.
2. XYY = assembly and date code.
3. Sample stock is generally held on part numbers listed in **BOLD**.
4. Available exclusively outside of the United States and its territories.
5. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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